CHANNEL COLLECTOR TRANSISTOR

The Government has rights in this invention persuant to Grant GK 39890 awarded by the National Science Foundation.

This is a continuation of Ser. No. 06/148,471, filed May 9, 1980, now abandoned, which was a continuation of Ser. No. 05/799,530, filed May 23, 1977, now abandoned.

CROSS-REFERENCES

To the extent used herein, teachings of U.S. Pat. No. 3,404,295 to R. M. Warner Jr., dated Oct. 1, 1968, with respect to the use of "lock-layer" principles in transistor design, are expressly herein incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention:

This invention relates generally to electronic solid-state amplifier devices, and more particularly to such a device which integrates bipolar junction transistor, field-effect transistor and lock-layer transistor principles in a single solid-state structure having advantages over devices employing only one or two of these component transistor principles.

2. Description of the Prior Art:

Since its inception, the bipolar transistor has become the "work horse" of the microelectronics industry, with relatively few basic improvements besides those relating to fabrication and processing (which have applied to the entire microelectronics and solid-state devices industry). One shortcoming of the conventional bipolar transistor structure was the fact that improvement in current gain of the device typically required reducing the metallurgical base thickness and "doping", which in turn directly limited the upper voltage rating of the transistor. In such devices, as increased voltage is applied to the collector of the transistor, the space-charge region associated with the collector junction expands in response to the increased voltage and extends farther into both the collector region and the base region of the transistor. While the expanded space-charge region has a relatively unimportant effect in the collector region of the transistor, it has a marked influence on transistor properties in the base region for the following reasons. It diminishes the effective base thickness, thus increasing the current gain of the transistor which in turn degrades the output impedance of the (common emitter) transistor, and it causes a voltage feedback from the output to input terminals of the transistor. This combination of phenomena is well known in the art as the "Early effect".

Initial efforst in minimizing the Early effect and in achieving high breakdown voltage led to what is known in the art as the "intrinsic-barrier" structure which was later replaced by the "mesa" transistor which incorporated base-diffusion principles that were relatively simple to implement. In both cases, a lightly doped collector region and a heavily doped base region caused the space charge region to thicken preferentially on the collector side of the collector-base junction. While present designs of high-voltage, high-current gain transistors have improved significantly over the first such base-diffused transistors, the general design principles remain the same, requiring the designer to trade off current gain against the voltage rating of the transistor.

U.S. Pat. No. 3,404,295, by Warner, one of the co-inventors of this invention discloses a more recent prior art transistor structure which sought to minimize the Early effect, and increase breakdown voltage by use of a "lock-layer". The so-called lock-layer transistor operates to diminish or to eliminate the dependency of the active base thickness on collector-base voltage by burying an opposite conductivity-type region (i.e. the lock-layer) in the collector body portion of the transistor and by reverse biasing its junction. The lock-layer transistor concept was originally based on the principle that one space-charge region can "lock" the dimensions of another region that is sufficiently close to it. This principle can be illustrated by considering a three-region structure. To create locking, two junctions are formed very close to one another by placing a thin opposite-type layer between two like-type regions. By establishing a fixed potential difference (zero volts being acceptable) between the two like-type regions and by reverse biasing both junctions, a condition can be created such that the space-charge regions thus created touch one another. Once this occurs, additional increases in either reverse biase will not affect the dimensions of the space-charge regions in those portions of the device where they interact. An explanation of this phenomenon is that the two junctions "compete" for the ionic charge in the thin layer between them. Once that ionic charge is consumed in their respective space-charge regions, the two "double-layers" of charge have dimensions that are fixed or "locked". Therefore, if a junction of limited lateral extent is placed close to a larger plane junction and locking is established, the space-charge region of the plane junction will exhibit an indentation on its "far side". In other words, space-charge region increments associated with further voltage increases are "transplanted" to a location down inside the collector body, where their effects are minimal.

In the above-reference patent 3,404,295, the lateral extent of the "lock-layer" was restricted to approximately underlie the emitter region of the transistor. Such devices are not very effective in minimizing the Early effect, are not very effective in raising breakdown voltage, and are also difficult to fabricate.

An attempted improvement upon the Warner patent is disclosed in U.S. Pat. No. 3,564,356 to Wilson. Wilson discloses a high-voltage integrated circuit transistor that employs a collector region which is characterized by virtually complete depletion of majority carriers at a collector-emitter voltage which is less than the voltage at which the collector-emitter breakdown would otherwise occur. As a result of this depletion, the effective collector-emitter breakdown voltage of the resultant device is increased since the field intensity in the collector-base space-charge region is limited. It is a fact that transistors of this kind do not exhibit complete depletion of the collector region when operated at useful (non-zero) current levels. Wilson did not recognize this fact or the closely related fact that a thin collector region actually comprises the channel of a JFET. The channel region of a JFET at nonzero current is characterized by the condition of quasineutrality. Because Wilson did not recognize the presence of a JFET, he did not extend his analysis to include teachings of "merging" other active devices into the design of his basic transistor configuration, as is the intent of this invention. Accordingly, neither the Wilson structure nor his processing considerations recognize or teach the unique "integrated